

What is claimed is:

1. A full depletion SOI-MOS transistor comprising:
 - a substrate having a main surface;
 - a buried oxide layer formed on the main surface of the
 - 5 substrate;
 - a thin silicon layer formed on the buried oxide layer,
 - the thin silicon layer including a channel region and a
 - source/drain region;
 - an isolation layer formed on the buried oxide layer, the
 - 10 isolation layer surrounding the thin silicon layer;
 - a gate insulation layer formed on the channel region of
 - the thin silicon layer;
 - a gate electrode formed on the gate insulation layer;
 - and
 - 15 a polysilicon layer formed on the source/drain region
 - of the thin silicon layer.
2. A full depletion SOI-MOS transistor according to claim 1, further comprising a sidewall formed on the gate insulation layer, wherein the sidewall surrounds the gate
- 20 electrode.
3. A full depletion SOI-MOS transistor according to claim 1, wherein the polysilicon layer extends on the isolation layer.
4. A full depletion SOI-MOS transistor according to claim 2, wherein the polysilicon layer extends on the sidewall.
- 25 5. A full depletion SOI-MOS transistor according to claim

1, wherein a thickness of the thin silicon layer is about 20 to 80 percent of a total thickness of the thin silicon layer and the polysilicon layer.

6. A full depletion SOI-MOS transistor according to claim 1, wherein a thickness of the thin silicon layer is about less than 35 nm.

7. A full depletion SOI-MOS transistor comprising:
a substrate having a main surface;
a buried oxide layer formed on the main surface of the substrate;
a thin silicon layer formed on the buried oxide layer, the thin silicon layer including a channel region and a source/drain region;

an isolation layer formed on the buried oxide layer, the isolation layer surrounding the thin silicon layer;

a gate insulation layer formed on the channel region of the thin silicon layer;

a gate electrode formed on the gate insulation layer;
and

a silicide layer formed on the source/drain region of the thin silicon layer and the gate electrode.

8. A full depletion SOI-MOS transistor according to claim 7, further comprising a sidewall formed on the gate insulation layer, wherein the sidewall surrounds the gate electrode and silicide layer formed thereon.

9. A full depletion SOI-MOS transistor according to claim 7, wherein the silicide layer formed on the source/drain region extends on the isolation layer.

10. A full depletion SOI-MOS transistor according to claim 8, wherein the silicide layer formed on the source/drain region extends on the sidewall.

11. A full depletion SOI-MOS transistor according to claim 7, wherein a thickness of the thin silicon layer is about 20 to 80 percent of a total thickness of the thin silicon layer and the silicide layer formed on the source/drain region.

12. A full depletion SOI-MOS transistor according to claim 7, wherein a thickness of the thin silicon layer is about less than 35 nm.

13. A full depletion SOI-MOS transistor comprising:
a substrate having a main surface;
a BOX layer formed on the main surface of the substrate;
an SOI layer formed on the BOX layer, the SOI layer including a channel region and a source/drain region;
an isolation layer formed on the BOX layer, the isolation layer surrounding the SOI layer;
a gate insulation layer formed on the channel region of the SOI layer;
a gate electrode formed on the gate insulation layer;
and
a high mobility conductive layer formed on the

source/drain region of the thin silicon layer, the high mobility conductive layer containing polysilicon.

14. A full depletion SOI-MOS transistor according to claim 13, further comprising a sidewall formed on the gate insulation layer, wherein the sidewall surrounds the gate electrode.

15. A full depletion SOI-MOS transistor according to claim 13, wherein the high mobility conductive layer extends on the isolation layer.

10 16. A full depletion SOI-MOS transistor according to claim 14, wherein the high mobility conductive layer extends on the sidewall.

17. A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is about 20 to 80 percent of a total thickness of the SOI layer and the high mobility conductive layer.

18. A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is about less than 35 nm.

20 19. A full depletion SOI-MOS transistor according to claim 13, wherein the high mobility conductive layer contains silicide.

20. A full depletion SOI-MOS transistor according to claim 19, wherein the high mobility conductive layer is formed on the gate electrode.